PH Sensing Using Ion Sensitive Field Effect Transistors: Undergraduate Laboratory Experiment

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An ion-sensitive field effect transistor is a still-developing technology in the biomedical field, having exciting lab-on-a-chip applications. Acting similar to a MOSFET, the ISFET can change electrical properties based on the pH of a liquid being sensed. This paper outlines a potential process allowing undergraduate students access to the design, manufacturing, and testing of these types of devices. . This gives students hands-on experience with state-of-the-art technology, and practical experience that transitions smoothly into industry . Successful students in this laboratory will have extended their theoretical knowledge into physical form, learning about practical constraints and testing protocols. This report follows one example group through the 12-week process. The final device was successful, exhibiting a change in electronic behaviour depending on the pH of the solution being sensed.

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I. INTRODUCTION

Ion sensitive field effect transistors are a novel type of sensors that are based on the MOSFET strusture. Typically, a MOSFET will have a source, drain, and gate region. Ideally, current passing between the source and drain can be altered according to the voltage applied at the gate. In the same way, ISFETs have a source and drain, but instead of a metal-oxide gate, there is a sensing layer that interacts with a solution that is in contact with the sensing gate . This layer, typically silicon nitride, interacts with the hydrogen ions in the solution, and changes the capacitance according to the strength of the pH in the solution. The equation shown in 1 outline the theoretical threshold voltage of the device. As can be seen, one of the factors in this equation relates to the pH[1]. These devices are part of an emerging field of possible lab-on-a-chip opportunities, as the pH of bodily fluids can help with quick disease diagnosis.[1]

$$V_{T_{isfet}} = E_{ref} + \chi_{sol} - \frac{2.3kT}{q}\left(\frac{\beta}{\beta+1}\right)(pH_{pzc} - pH) + V_T \quad (1)$$

On top of this, these devices can be made using standard semiconductor manufacturing techniques, using a relatively small number of masks and processing steps. Graduating students in the fields of physics, engineering, and biomedical research could benefit greatly from this kind of experience. In this example, fourth year engineering students

II. EXPERIMENTAL DETAILS

A. ISFET Research and Design

The first aspect of this project is for students to research the theory behind ISFETs. At this point, students are also arranged into groups of 2 to 4 according to the availabilty of their schedules and laboratory. Two weeks after the course begins, each group is required to present their design for their unique ISFET. If the designs are deemed reasonable by the professor and lab technician, the groups can proceed with the manufacturing. If not, they must to make the appropriate revisions before continuing.

Before beginning any manufacturing toward a final device, all students must demonstrate a cursory knowledge of theory behind an ISFET device. The requirements for the preliminary design include a brief introduction outlining the functioning of the device, autoCAD sketches showing the details of the masks, and justification for each of the features. Additional deliverables in this section include the masks that will be used, a side-view representation of the final device, and a process flow diagram outlining each of the steps to be taken

On top of this , groups also have to prepare for the manufacturing steps by calculating the thicknesses of each layer for a desired turn-on voltage. All of the above information must be presented to the lab staff before coninuing on to the manufacturing.

B. Experimental Procedure

After the design component was approved, the groups move on to the manufacturing of the device. Outlined below are each of the processes that the example group followed. This order may change depending on the design and process flow that the group chose, but the techniques will be similar. Other differences between groups include timing, density, dose, and material. For all groups, 4 masks must be designed and printed. The methods below outline all of the manufacturing steps taken before each mask was used as well.

1. Mask 1

After receiving a fresh, blank wafer, the students cleaned it using a standard procedure involving buffered HF and H2SO4[2].

After the wafer is clean, the first layer of silicon dioxide can be grown. This is done in the furnace located in the lab. The thickness of the SiO_2 layer depends on the amount of time it is in the furnace, and therefore needs to be calculated by the students beforehand. The rate of growth can also be changed by the temperature of the oven. In this case, the maximum temperature was 1100 ° C. The wafer was placed in the oven at 950 ° C, for 7.25 minutes to grow about 40 nm of SiO_2.

Next, a layer of silicon nitride is needed. This will eventually act as the sensing layer, and the thickness is important. Once again, this is a process that required previous investigation to know for how long to sputter the nitride onto the surface of the wafer. Due to the difficult nature of the sputtering process, this step was done by the laboratory staff.

After this, the first mask can be used to isolate the future source and drain regions. These need to be isolated in order to dope them using ion implantation later on. Figure 1 shows the first mask used. As can be seen, the source and drain regions are elongated to allow for a seperation between the sensing layer and the contact pads. This is required because if the solution being sensed was also in contact with the pads, a short circuit would be created, and the entire transistor would not function.

The procedure for putting the mask on, exposing it, and removing it is outlined below. For the future masks, these details will not be restated, since the process is the same First, a layer of photoresist is spin-coated onto the substrate. This step may or may not involve primer, depending on the type of photoresist being used. Students should know the different types of photoresist available, and when to use them. It is important in this step that the students cover the entire wafer, as evenly as possible. After spinning, the mask can be aligned onto the wafer. Alignment markers were added to the masks to help with this process, also seen in figure 1. A mislaid mask could greatly influence the future performance of the device. Once again, due to the difficult and precise nature of this task, it was performed by lab staff. After the mask is properly laid, the exposure can take place.

2. Mask 2

After the mask exposure, before doping the source and drain regions, the silicon nitride and silicon oxide layers must be removed. The nitride layer is done through a reactive ion etch, performed by the lab staff. After this , the oxide layer can be removed by an HF etch, performed by the students[2]. At this point, the bare wafer is exposed in both the source and drain regions. The photoresist can be washed off at this point, since the oxide and nitride layers are protecting the rest of the wafer. This removal of photoresist is done by a simple acetone bath, followed by a rinse in DI water.

FIG. 1.
Mask 1 blocks the entire wafer, except for the source and drain regions. This iamge shows only one corner of the entire wafer. In total there are 16 devices, all with similar structure.

FIG. 2.
Mask 2 blocks only the sensing regions. This allows the silicon nitride to be removed, creating the proper double-stack layer needed for the pH sensing over the gate.

These source and drain regions now need to be highly doped, creating a channel, allowing for current to pass through the wafer easily. To do this, ion implantation of the regions was performed by the lab staff. Students were required to indicate the specific ions, energy, dose, diffusion temperature and diffusion time for this implantation process according to the calculated profile found during the research phase. These can be calculated based on the desired depth of the channel, the dopant profile, and the type of substrate. In this case, phosphorous ions were implanted at 35 keV, at a dose of 1e18 ions/cm^2. The diffusion temperature was 1100 C °, for 25 minutes.

The wafer can now be prepared for the second mask, shown in figure 2. For this mask, the sensing layer is isolated, ensuring that the nitride layer is only present over the gate region.

3. Mask 3

After the second mask is aligned and exposed, the oxide and nitride needs to be removed from the wafer, followed by the photoresist. This is done in the same way as before, with a buffered HF solution, reactive ion etching, acetone, and DI water[2].

After everything is removed, the passivation layer of

FIG. 3.
Mask 3 blocks the entire wafer except for the contact regions. The silicon dioxide needs to be removed from these regions in order to form good ohmic contacts when testing.

silicon dioxide needs to be grown over the entire device, except for the sensing regions. This means that the same mask can be used, and the wafer in its current state is appropriate. Similar to before, the silicon dioxide is grown in a tube furnace. The passivation layer thickness is not as important as the other layers, but the students should grow at least 200 nm. This ensures that the solution will only be in contact with the sensing region, and will not influence the performance of the device by causing a short-circuit.

Now that the doiuble stack layer is created, and the passivation layer is grown, the third mask, figure 3, can be aligned. This mask exposes the contact regions for a silicon dioxide etch.

4. Mask 4

Before the fourth mask, the passivation layer must be removed from the contact regions isolated by mask 3. This can be done using the same HF etching procedure used for past SiO_2 layers, except it will need to be done for a longer time. It is important to avoid etching too long in this suituation, as this will lead to sideways etching instead on downward.

After this, the fourth and final mask, seen in figure 4, can be aliigned. This mask also outlines the contact regions for aluminum deposition. This may seem like a trivial step, but the contact regions are slightly larger in this step compared to the last. This is important, as it ensures that the contact regions are fully covered, and the aluminum can creates the most contact possible. On top of this, a larger contact region is easier for the experimenter when testing the device.

5. Final Steps

After the final mask is in place, the aluminum deposition can be performed. This process, performed by lab staff, coats the entire wafer with about 250 nm of aluminum. Once this is in place, the photoresist can be re-

FIG. 4.
Mask 4 is similar to mask 3, except the regions are larger to ensure good coverage, and make contact with the testing probes easier.

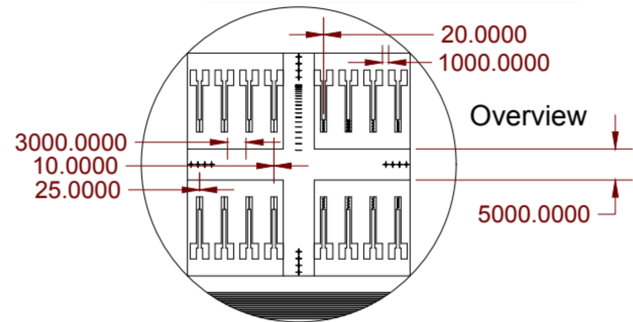

FIG. 5.
This wafer was made with 8 unique devices on it. Each device has a unique W/L ratio, so that the relationship between this ratio and the device performance can be tested as well.

moved through a sonication process, by shaking the wafer in an acetone, isopropanol, and DI water. This process will remove the photoresist, as well as any aluminum sitting on top of it As mentioned earlier, this will result in aluminum covering the entire contact areas, but nowhere else. Once this is complete, annealing can take place. This heating sets the aluminum in place and ensures an ohmic contact on the contact pads.

Once the annealed wafer is cool, the prodecure is complete, and the ISFETs ready to be tested. On the example wafer, 8 devices were built, each having a unique ratio between channel length and width. This can be seen in figure 5. This was done to open the possibility of further testing on the size of the response as a function of the W/L ratio. These results are not included in this paper. To avoid having manufacturing errors negating any results, each of the devices were built twice, mirrored on the chip. This mirroring could also be used for consistency testing later on. In total, 16 ISFETs were fit onto one wafer, with room to spare.

III. RESULTS AND DISCUSSION

A. Testing

Ideally, each of the devices will be tested using multiple solutions of a different pH. Due to time and resource

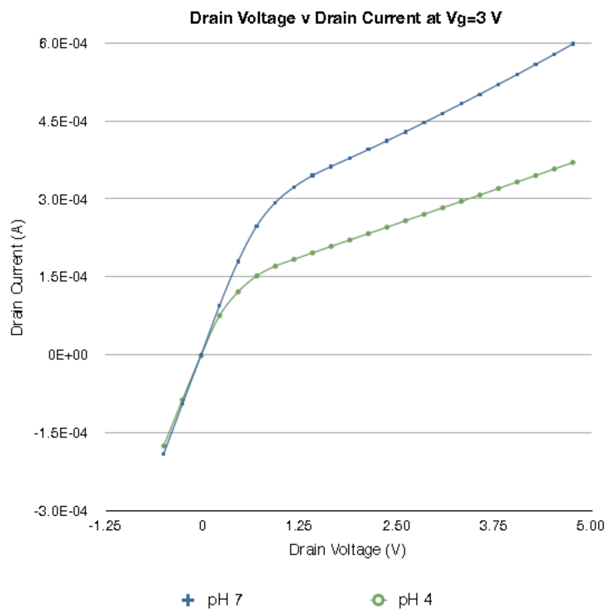

FIG. 6.
A sample of the type of charts that a successful device should achieve. As the pH of the solution changes, the response of the ISFET is influenced.

constraints, each group should have at least one or two tested using DI water and a known pH solution. As discussed earlier, it is important that for each test, the solution only contacts the sensing region, and both source and drain probes are making good contact with the pads. Lastly, the reference electrode needs to be submerged in the solution. If these conditions are met, standard transistor testing procedures can be performed, ie: ohmic contact test, pn junction quality test, and IV characteristic curves.

B. Results

For the example group outlined in this paper, multiple devices were tested. In general, good ohmic contacts were seen for all of the pads, and typical MOSFET behaviour was shown.

To test the relationship with pH, the device with the best ohmic behaviour at the pads was chosen. The threshold voltage was found using water and a solution with a pH was 7. These results can be seen in figure 6

This relationship should be further investigasted by the student groups in their final report. As briefly mentioned , each of the devices on this wafer had a different W/L ratio, and this can be investigated as well.

C. Discussion

The key finding for this report should include a measureable change in threshold voltage based on the pH of the solution being sensed. Whether or not this is successful though, the laboratory components allowing students to perform the industry-standard manufacturing steps is important. If the devices are not successful, students may be able to use specific examples of errors made in these steps to explain the malfunction.

While the process outlined in this paper can create a functional device, specific procedure could change depending on the process flow designed by the group. The common feature between all groups is that 4 masks were used. In terms of the success of this example, the device did exhibit a relationship with the solution sensed. However, the theory did not predict this behaviour exactly. For further developments, this theory should be investigated further in order to properly predict the behaviour of the device.

Provided students attend all of the laboratories, they will gain first-hand knowledge on the operation of many of the pieces of equipment used to make these devices. It is important, expecially for the steps performed by lab staff, that the students are aware of how the equipment is being used and relative safety measures that need to be implemented. Ideally, the students will have a chance to see all of the equipment, even if they cannot operate it themselves. Ideally, these eqperiences will be used to entice employers to hire them, as they already have experience with working with these kinds of devices.

IV. CONCLUSION

Overall, this paper outlines a clear method for the manufacturing of an ion-sensitive field effect transistor, which can be performed by an undergraduate design team. This project requires the proper equipment and materials in the lab, as well as properly trained staff. In the first year of running this course, most groups were able to create multiple functioning devices on a single wafer.

The important aspect of this project is that it provides an avenue for undergraduate students to get hands-on experience with practical and industry-standard techniques in the field of semiconductor manufacturing. This unique opportunity creates an advantage for graduates entering into the field, as the have experience, background knowledge and a taste of the work environment.

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